



19" XFFTS crate equipped with eight XFFTS boards and one XFFTS controller

Each XFFTS-board operates from a single 5 Volt source and dissipates less than 30 Watt, depending on the actual configuration in terms of bandwidth and number of spectral channels. Precise time stamping of the processed spectra is realized by an on-board GPS/IRIG-B time decoder. Furthermore, the 10-layer boards include a programmable ADC clock synthesizer for a wide range of configurations (bandwidth: 0.1 – 2.5 GHz), making the spectrometer flexible for different observation requirements.

The XFFTS-boards include a standard 100 MBit/s Ethernet interface, which simplifies the combination of many boards into an Array-XFFTS, simply by integration of a common buffered Ethernet switch. Up to eight XFFTS-boards can be housed in one XFFTS-crate together with power supplies (4 × 5 Volt / 20 Amperes) and one XFFTS-controller.

The XFFTS-controller manages the synchronization of the XFFTS-boards. It provides a reference clock for the on-board ADC synthesizers or the GPS/IRIG-B timing information. In addition, the XFFTS-controller displays housekeeping information on a four line LCD, like board IP numbers, temperatures of the ADC and FPGA chips as well as the power level of the IF inputs.

TECHNICAL DATA

Signal Input

Full Power Bandwidth (-3 dB)	0.1 GHz to 2.5 GHz (for further details contact RPG)
Input Power	full scale input power: -2 dBm (500 mVpp)
Max. Input Voltage	±2 VDC
Impedance	50 Ω
Input Coupling	AC (Balun)
Input Isolation (I/Q) @ 2.6 GHz	> 60 dB (channel-to-channel)
Input Connector	SMA (gold plated)



Digital Conversion

ADC Type	E2V EV10AQ190
Sample Rate	up to 5 GSPS
ADC Resolution	10 bit (-512 to +511)
ENOB, full bandwidth	7.6 @ 620 MHz 7.2 @ 1200 MHz
SFDR (typical)	>57 dBc @ 620 MHz >55 dBc @ 1200 MHz
Differential Nonlinearity (typ.)	±0.3 LSB
Integral Nonlinearity (typ.)	±0.8 LSB

Reference Frequency Input (FFTS Controller)

Ext. Clock/Ref. Threshold	800 mVpp
Maximum Input Voltage	3.0 Vpp
Reference Frequency Range	5 to 250MHz (5MHz step size, programmable)
Input Connector	SMA (gold plated)

Time Base

Clock Accuracy	±50ppm (XFFTS Controller)
Sampling Jitter	< 500fs RMS (10µs record length)

On-Board GPS/IRIG-B Time Decoder

Standard	IRIG-B 12x, 1kHz, AM modulated
Accuracy (decoding)	< 50µs

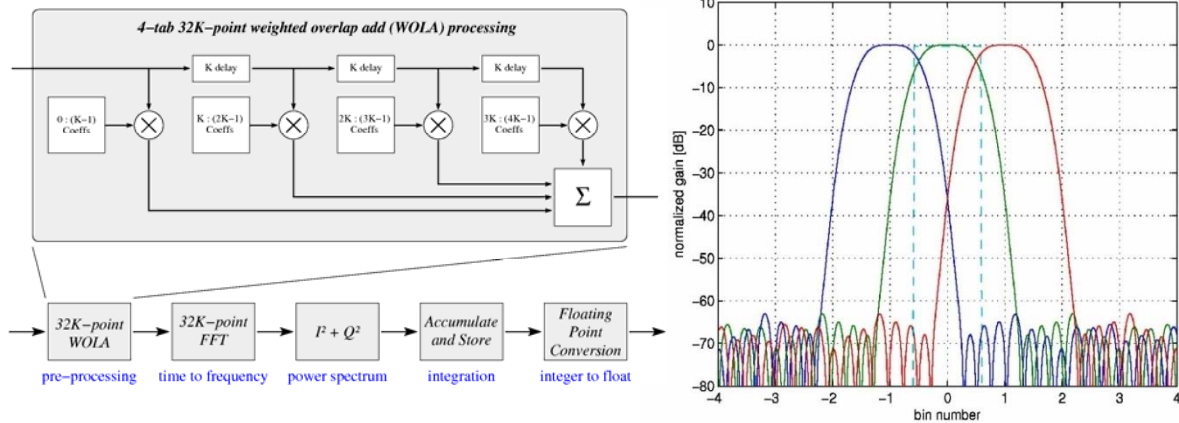
On-Board Ethernet Interface

Standard	IEEE 802.12 (100MBit/s)
Data Rate	80 Mbit/s, sustained

On-Board Data Processing Unit (DPU)

FPGA (main DPU)	XILINX Virtex-6 XC6VLX 240T
FPGA (Ethernet, etc.)	XILINX Spartan-3 XC3S 1000

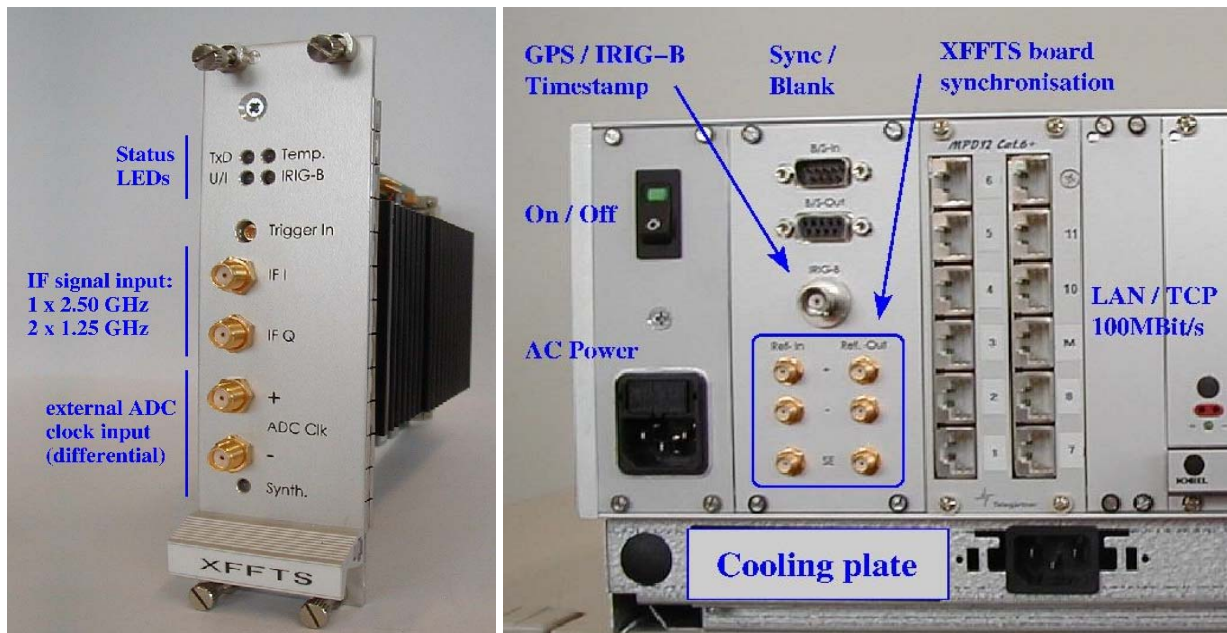
FPGA signal processing pipeline



Left: Block diagram of the 4-tap polyphase signal processing pipeline implemented in the XFFTS. **Right:** Frequency response of the optimized FFT signal processing pipeline. The diagram shows three adjacent frequency bins in logarithmic scale. The dashed lines illustrate the equivalent noise bandwidth (ENBW) for the corresponding spectral line.

(B. Klein, et al., 2008, 19th ISSTT, Groningen, B. Klein, et al., 2009, 20th ISSTT, Charlottesville, USA)

XFFTS Connectivity



General Specification

PC System Requirements

Processor (CPU)	Pentium 4 (2GHz or higher) Dual Core CPU recommended
Memory	1 GB RAM (more recommended when working with several XFFTS boards)
Operating System	Linux (Kernel 2.6)
Hard Drive Space	min. 300 MB
Ethernet Switch	A managed Ethernet switch capable of buffering data for each Ethernet port is recommended.



Temperature

Environmental conditions (indoor use only)

Operating temperature range	0°C to 40°C
Storage Temperature	-30°C to 60°C
Operation Altitude	3000 m (contact RPG for further details)
Required Airflow	>2 m/s
Relative humidity	5-90% (non condensing)

Power supply

AC Supply	108 VAC to 120 VAC & 216 VAC to 240 VAC 50 Hz to 60 Hz (auto adjust)
Power Consumption	max. 200 W (depending on FPGA core version and operation mode); 4 internal power supplies 5VDC/20A
Dimensions (w x h x d)	480 x 135 x 485 mm 19" crate, 3 units height standard crate, rack mount
Weight	max. 13 kg